The opinion in support of the decision being entered today was not written for publication and is not binding precedent of the Board.

Paper No. 21

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte ZOHAR BOGIN, DAVID D. LENT and VINCENT VON BOKERN

Appeal No. 2003-0836
Application No. 09/205,086

ON BRIEF

Before JERRY SMITH, FLEMING and SAADAT, Administrative Patent Judges.

SAADAT, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal under 35 U.S.C. § 134 from the Examiner's final rejection of claims 1-28 and 38-49, which are all of the claims pending in this application. Claims 29-37 have been canceled.

We affirm.

BACKGROUND

Appellants' invention is directed generally to a memory controller including a refresh timing circuit that generates clock pulses (specification, page 4). An understanding of the invention can be derived from a reading of exemplary independent claim 1 and dependent claim 3, which are reproduced as follows:

1. A computer system comprising:

a memory; and

a memory controller, wherein the memory controller includes a refresh timing circuit for generating clock pulses used to trigger memory refresh events.

3. The computer system of claim 2, wherein the refresh timing circuit further comprises:

a clock generator for generating the clock pulses;

a first counter coupled to the clock generator;

a storage register coupled to the clock generator and the counter; and

a comparator coupled to the clock generator, the counter and the storage register.

The prior art reference of record relied upon by the Examiner in rejecting the appealed claims is:

Direct Rambus Technology Disclosure (DRTD), pgs. 1-16, (October 15, 1997).

Claims 1-28 and 38-49 stand rejected under 35 U.S.C. § 102(b) as being anticipated by DRTD.

We make reference to the answer (Paper No. 19, mailed November 15, 2002) for the Examiner's complete reasoning in support of the rejections, and to the appeal brief (Paper No. 18, filed October 15, 2002)for Appellants' arguments thereagainst. Only those arguments actually made by Appellants have been considered in this decision. Arguments which Appellants could have made but chose not to make in the brief have not been considered. See 37 CFR 1.192(a).

CLAIM GROUPINGS

Appellants state their intention to have claims 1, 2, 15 and 16 stand or fall together as Group I and claims 3-14, 17-27 and 28-49 stand or fall together as Group II. In accordance with this grouping, and pursuant to 37 CFR § 1.192(c)(7), we will limit our review to claim 1 for Group I, and claim 3 for Group II.

OPINION

While the Examiner has not specifically indicated that the 35 U.S.C. § 103 rejection is withdrawn, only a 35 U.S.C. § 102(b) rejection remains in the final Office action (Paper No. 13, mailed April 18, 2002) for all the appealed claims. Appellants properly appealed this rejection and provided relevant arguments in their brief. The Examiner's attempt to revive a previously

applied rejection in the answer, which was not included in the final Office action, constitutes a new ground of rejection. This is not permitted under 37 CFR 1.193(a)(2) as explained in MPEP 1208.01. It is also unclear to us why Appellants chose not to file a reply brief in view of the new ground of rejection in the Examiner's answer. However, for the purpose of this appeal, we will only consider the 35 U.S.C. § 102(b) rejection which was maintained by the Examiner in the final Office action.

With respect to the 35 U.S.C. § 102(b) rejection of claims 1-28 and 38-49, Appellants argue that DRTD lacks a "refresh timing circuit for generating clock pulses used to trigger memory refresh events" (brief, page 6). Appellants acknowledge that DRTD describes a memory controller that only "supports" refreshes (DRTD, page 14), but does not "generate" clock pulses used to trigger these memory refreshes (brief, page 6). Appellants further assert that although the Rambus Memory Controller (RMC) may "control" refreshing, no timing circuitry is disclosed that "generates" these clock pulses (brief, page 7). Specifically, Appellants argue that the RMC receives external clock pulses to trigger a memory refresh (brief, page 7), thus requires an additional pin which may lead to an increase in circuit complexity.

In response, the Examiner argues that the RMC is a controller for dynamic RAM (DRAM) which inherently requires refreshing to maintain coherency of the stored data (answer, page 7). Examiner further states that the RMC can include an internal clock generator (answer, page 4).

A rejection for anticipation under section 102 requires that the four corners of a single prior art document describe every element of the claimed invention, either expressly or inherently, such that a person of ordinary skill in the art could practice the invention without undue experimentation. See Atlas Powder Co. V. Ireco Inc., 190 F.3d 1342, 1347, 51 USPQ2d 1943, 1947 (Fed. Cir. 1999); In re Paulsen, 30 F.3d 1475, 1478-79, 31 USPQ2d 1671, 1673 (Fed. Cir. 1994).

A review of DRTD reveals that the reference relates generally to DRAM, memory controllers and a bus structure (DRTD, page 7). The reference explicitly teaches that the RDRAMs only respond to requests, and the RMC is the only device that generates these requests (id.). Therefore, the RMC generated request signals must include these refresh signals. Although the reference in Figure 4 on page 8 shows that the RMC is connected to an external clock, the reference on page 9 also discloses an internal clock that "can be integrated in the memory controller."

We also note Appellants' argument that a memory controller (MC) doesn't inherently include a refresh timing circuit. Appellants specifically argue that:

> In fact prior art memory controllers, such as the RMC disclosed in *the Rambus Disclosure*, receive clock pulses from an external clock source in order to trigger a memory refresh.
> (brief, page 7).

This argument attempts to differentiate between implementing internal and external clock sources. Not only does the reference explicitly state, as discussed above, that the RMC may contain an internal clock source, but also Appellants' invention does appear to include an external clock in addition to an internal clock source to trigger a memory refresh. In fact, in contradiction to Appellants' own argument, the claimed invention's internal clock generator [432] is disclosed to utilize an external clock source (labeled as host clk) in order to trigger a non-sleep memory refresh instead of the already present internal clock source (labeled as osclk) (Figs. 4, and 8; specification, pages 10, 11 and 14).

Therefore, we are unpersuaded by Appellants' argument that the timing circuitry in the RMC does not generate the timing refresh pulse used to trigger memory refresh events. As established above, the only requests received by the RDRAM are

generated by the RMC which may include an internal clock. Further, the fact that DRTD discloses that the RMC supports all the control functions, including refresh (right-column, page 14), does not preclude having the refresh timing circuit as an internal part of the RMC.

Based on our findings above, we agree with the Examiner that the reference DRTD anticipates the claimed subject matter in the exemplary independent claim 1 for Group I. Accordingly, we sustain the 35 U.S.C. § 102(b) rejection of claims 1, 2, 15 and 16.

Regarding claim 3, in addition to the arguments made above, Appellants contend that DRTD fails to disclose a refresh timing circuit with an internal clock generator, a counter, a storage register or a comparator. Appellants rely on the same arguments that were provided for Group I and merely list the additional limitations found in claim 3. These statements are conclusory rather than substantive. "A general allegation that the claims define a patentable invention without specifically pointing out how the language of the claims patentably distinguishes them from the references does not comply with the requirements of this section" 37 CFR § 1.111(2)(b). As discussed above, with respect to Group I, DRTD does explicitly disclose a refresh timing

circuit with an internal clock generator and therefore anticipates claim 3. Accordingly, the 102(b) rejection of claims 3-14, 17-27 and 38-49 is sustained.

CONCLUSION

To summarize, the decision of the Examiner to reject claims 1-28 and 38-49 under 35 U.S.C. § 102 is affirmed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136 (a).

AFFIRMED

JERRY SMITH
Administrative Patent Judge

MICHAEL R. FLEMING
Administrative Patent Judge

MAHSHID D. SAADAT
Administrative Patent Judge

BOARD OF PATENT APPEALS AND INTERFERENCES

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